TRANSMITTAL FORM

Application Serial Number	10/688,003
Filing Date	October 17, 2003
First Named Inventor	Hammond
Group Art Unit	2811
Examiner Name	Not Yet Available
Attorney Docket No.	ASC-001C1
Patent No.	Not Applicable
Issue Date	Not Applicable

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Check Attached
  - ☐ Copy of Fee Transmittal Form
- ☐ Amendment/Response
  - ☐ Preliminary
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
  - ☐ Letter to Official Draftsperson including Drawings [Total Sheets _____]
- ☐ Petition for Extension of Time
- ☒ Supplemental Information Disclosure Statement
  - ☒ Form PTO-1449
  - ☒ Copies of IDS Citations B1-B8 and C5-C83
- ☐ Certified Copy of Priority Document(s)
- ☐ Sequence Listing submission
  - ☐ Paper Copy/CD
  - ☐ Computer Readable Copy
  - ☐ Statement verifying identity of above
- ☐ Copy of Notice to File Missing Parts of Application
- ☐ Formal Drawing(s)
- ☐ Request For Continued Examination (RCE) Transmittal
- ☐ Power of Attorney (Revocation of Prior Powers)
- ☐ Terminal Disclaimer
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- ☐ Small Entity Statement
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- ☐ Notice of Appeal to Board of Patent Appeals and Interferences
- ☐ Appeal Brief (in triplicate)
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- ☒ Return Receipt Postcard
- ☒ Certificate of First Class Mailing under 37 C.F.R. 1.8
- ☐ Certificate of Facsimile Transmission under 37 C.F.R. 1.8
- ☐ Additional Enclosure(s) *(please identify below)*

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Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Hammond *et al.*		
SERIAL NO.:	10/688,003	GROUP NO.:	2811
FILING DATE:	October 17, 2003	EXAMINER:	Not Yet Assigned
TITLE:	BACK-BIASING TO POPULATE STRAINED LAYER QUANTUM WELLS		

CERTIFICATE OF FIRST CLASS MAILING UNDER 37 C.F.R. 1.8

I hereby certify that this correspondence, and any document(s) referred to as enclosed herein, is/are being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 23rd day of February, 2004.

Emily Walsh

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith are:

1. Transmittal Form (1 page);
2. Supplemental Information Disclosure Statement (2 pages);
3. Form PTO-1449 (7 pages);
4. Copies of Cited References B1-B8 and C5-C83;
5. Return Receipt Postcard.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Hammond *et al.*		
SERIAL NO.:	10/688,003	GROUP NO.:	2811
FILING DATE:	October 17, 2003	EXAMINER:	Not Yet Assigned
TITLE:	BACK-BIASING TO POPULATE STRAINED LAYER QUANTUM WELLS		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with the provisions of 37 C.F.R. 1.97 and 1.98, Applicants hereby make of record the patents and publications listed on the accompanying Form PTO-1449, and other information contained herein, for consideration by the Examiner in connection with the examination of the above-identified patent application. In accordance with the U.S. Patent Office's partial waiver of the requirement under 37 C.F.R. 1.98(a)(2)(i), only copies of the foreign patent documents and non-patent publications are enclosed.

REMARKS

In accordance with the provisions of 37 C.F.R. 1.97, this statement is being filed (CHECK ONE):

☒ (1) within three (3) months of the **filing date** of a national application other than a continued prosecution application under 37 C.F.R. 1.53(d), or within three (3) months of the **date of entry of the national stage** as set forth in 37 C.F.R. 1.491 in an international application, or before the mailing of the **first Office action** on the merits, or before the mailing of a **first Office action** after the filing of a request for continued examination under 37 C.F.R. 1.114; or

☐ (2) after the period defined in (1) but before the mailing date of a **final action** or a **notice of allowance** under 37 C.F.R. 1.311, and

☐ the requisite Statement is below, **OR**

☐ the requisite fee under 37 C.F.R. 1.17(p), namely **$180.00**, is included herein, or

☐ (3) after the mailing date of a **final action** or **notice of allowance** but before the payment of the **issue fee, AND**

☐ the requisite Statement is below, **AND**

☐ the requisite petition fee under 37 C.F.R. 1.17(p), namely **$180.00** is included herein.

It is respectfully requested that each of the patents and publications listed on the attached Form PTO-1449, and other information contained herein, be made of record in this application.

Applicants believe that no fees are due for this paper to be entered and considered, but the Commissioner is hereby authorized to charge Deposit Account No. 20-0531 for any required fees that may be due.

Respectfully submitted,

Date: February 23, 2004
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FORM PTO - 1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-001C1 APPLICANT(S): Hammond *et al.* SERIAL NO.: 10/688,003 FILING DATE: October 17, 2003 GROUP: 2811

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A13	2002/0008289	01/24/2002	Murota *et al.*			
	A14	2002/0030203	03/14/2002	Fitzgerald			
	A15	2002/0104993	08/08/2002	Fitzgerald *et al.*			
	A16	2002/0123167	09/05/2002	Fitzgerald			
	A17	2002/0123183	09/05/2002	Fitzgerald			
	A18	2002/0125497	09/12/2002	Fitzgerald			
	A19	2003/0013323	01/16/2003	Hammond *et al.*			
	A20	2003/0052406	03/20/2003	Lochtefeld *et al.*			
	A21	2003/0077867	04/24/2003	Fitzgerald			
	A22	2003/0102498	06/05/2003	Braithwaite *et al.*			
	A23	2003/0207571	11/06/2003	Fitzgerald *et al.*			04/23/2003
	A24	4,212,019	07/08/1980	Wataze *et al.*			
	A25	4,771,013	09/13/1988	Curran			
	A26	5,101,254	03/31/1992	Hamana			
	A27	5,244,749	09/14/1993	Bean *et al.*			
	A28	5,331,185	07/19/1994	Kuwata			
	A29	5,461,245	10/24/1995	Gribnikov *et al.*			
	A30	5,548,138	08/20/1996	Tanimoto *et al.*			
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	A32	5,780,922	07/14/1998	Mishra *et al.*			
	A33	5,789,799	08/04/1998	Voinigescu *et al.*			
	A34	5,898,342	04/27/1999	Bell			

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-001C1 APPLICANT(S): Hammond *et al.* SERIAL NO.: 10/688,003 FILING DATE: October 17, 2003 GROUP: 2811

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	A35	6,052,380	04/18/2000	Bell			
	A36	6,111,267	08/29/2000	Fischer *et al.*			
	A37	6,111,367	08/29/2000	Asano *et al.*			
	A38	6,140,687	10/31/2000	Shimomura *et al.*			
	A39	6,160,274	12/12/2000	Folkes			
	A40	6,271,726	08/07/2001	Fransis *et al.*			
	A41	6,555,839	04/29/2003	Fitzgerald			
	A42	6,583,015	06/24/2003	Fitzgerald *et al.*			
	A43	6,593,191	07/15/2003	Fitzgerald			
	A44	6,593,641	07/15/2003	Fitzgerald			
	A45	6,646,322	11/11/2003	Fitzgerald			07/16/2001

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EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B1	01/93338 A1	12/06/2001	WO				N	Y
	B2	02/13262 A2	02/14/2002	WO				N	Y
	B3	02/071488 A1	09/12/2002	WO				N	Y
	B4	02/071491 A1	09/12/2002	WO				N	Y
	B5	02/071493 A2	09/12/2002	WO				N	Y
	B6	02/071495 A1	09/12/2002	WO				N	Y
	B7	02/103760 A2	12/27/2002	WO				N	Y
	B8	03/015138 A2	02/20/2003	WO				N	Y

EXAMINER	DATE CONSIDERED

FORM PTO - 1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-001C1 APPLICANT(S): Hammond *et al.* SERIAL NO.: 10/688,003 FILING DATE: October 17, 2003 GROUP: 2811

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.		OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
	C5	Abidi *et al.*, "Power-Conscious Design of Wireless Circuits and Systems," IEEE-2000, Vol. 88, Issue 10 (October 2000), pp. 1528-1545.
	C6	Abou-Allam *et al.*, "Impact of Technology Scaling on CMOS RF Devices and Circuits," IEEE 2000 Custom Integration Circuits Conference, (2000), pp. 361-364.
	C7	Aniel *et al.*, "Low Temperature Analysis of 0.25μm T-Gate Strained Si/Si0.55Ge0.45 N-MODFET's," IEEE, Vol. 47, Issue 7 (July 2000), pp. 1477-1483.
	C8	Ansley *et al.*, "Based Profile Optimization for Minimum Noise Figure in Advanced UHV/CVD SiGe HBTs," IEEE Transactions on Microwave Theory and Techniques, Vol. 46, No. 5 (May 1998), pp. 653-660.
	C9	Armstrong *et al.*, "Technology for SiGe Heterostructure-Based CMOS Device," PhD Thesis, Massachusetts Institute of Technology, 1999, pp. 1-154.
	C10	Assaderaghi *et al.*, "Current Status of Technology, Modeling, Design, and the Outlook for the 0.1 μM Generation," IEEE International SOI Conference 2000, (October 2000), pp. 6-9.
	C11	Borovitskaya *et al.*, "On Theory of 1/F Noise in Semiconductors," Solid-State Electronics, Vol. 45, Issue 7 (July 2001), pp. 1067-1069.
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	C13	Chatterjee *et al.*, "SUM-100NM Gate Length Metal Gate NMOS Transistors Fabricated by a Replacement Gate Process," IEEE, (1997), pp.1-4.
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	C17	Choi *et al.*, "A Low Noise On-Chip Matched MMIC LNA of 0.76DB Noise Figure at 5 GHz for High Speed Wireless LAN Applications," IEEE – GaAs IC Symposium, (2000), pp. 143-146.
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OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.		OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
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	C24	Frank *et al.*, "Device Scaling Limits of Si MOSFETS and their Application Dependencies," IEEE Proceedings, Vol. 89, Issue 3 (March 2001), pp. 259-288.
	C25	Gilbert *et al.*, "Analog at Milepost 2000: A Personal Perspective," IEEE-2001, Vol. 89, Issue 3 (March 2001), pp. 289-304.
	C26	Gray *et al.*, "Analysis and Design of Analog Integrated Circuits," John Wiley & Sons Publishing Co., Second Edition (1984), pp. 604-688.
	C27	Harame *et al.*, "Optimization of SiGe HBT Technology for High Speed Analog and Mixed Signal Applications," IEEE-IEDM 93 Conference, (December 1993), pp. 71-73.
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	C30	Huang *et al.*, "The Impact of Scaling Down to Deep Submicron on CMOS RF Circuits," IEEE Journal of Solid State Circuits, Vol. 33, Issue 7 (July 1998), pp. 1023-1036.
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	C33	Kim *et al.*, "A Fully Integrated 1.9GHz CMOS Low-Noise Amplifier," IEEE Microwave and Guided Wave Letters, Vol. 8, Issue 8 (August 1998), pp. 293-295.
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	C35	Klepser *et al.*, "A 10 GHz SiGe BiCMOS Phase-Locked-Loop Frequency Synthesizer," IEEE 2001 Custom Integrated Circuits Conference, (July 2001), pp. 567-570.
	C36	Koester *et al.*, "SiGe PMODFETs on Silicon-on-Sapphire Substrates with 116 GHz FMAX," IEEE Electron Device Letters, Vol. 22, Issue 2 (February 2001), pp. 92-94.
	C37	Konig *et al.*, "SiGe HBTs and HFETs," Solid-State Electronics, Vol. 38, Issue 9 (September 1995), pp. 1595-1602.
	C38	Kumar *et al.*, "A SOI/CMOS/BJT Technology for Integrated Power Amplifiers Used in Wireless Transceiver Applications," IEEE Electron Device Letters, Vol. 22, Issue 3 (March 2001), pp. 136-138.
	C39	Kumar *et al.*, "Novel Isolation Structures for TFSOI Technology," IEEE Electron Device Letters, Vol. 22, Issue 9 (September 2001), pp. 435-437.

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OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C40	Lagnado *et al.*, "RF Systems Based on Silicon-on-Sapphire Technology," IEEE – 2000 International SOI Conference, (October 2000), pp. 32-33.
	C41	Lagnado *et al.*, "Silicon-on-Sapphire for RF Si Systems 2000" IEEE – 2000 Topical Meeting on Digest of Papers, (2000), pp. 79-82.
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	C44	Larson *et al.*, "Manufacturing Study of Yield and Performance Dependence on Gate Length for Submicron Aniias-Gainas HEMT's," IEEE Transactions on Semiconductor Manufacturing, Vol. 6, No. 4 (November 1993), pp. 380-383.
	C45	Lee *et al.*, "CMOS RF Integrated Circuits at 5 GHz and Beyond," IEEE Proceedings, Vol. 88, Issue 10 (October 2000), pp. 1560-1571.
	C46	Lee *et al.*, "Strained Ge Channel P-Type Metal Oxide Semiconductor Field-Effect Transistors Grown in Si1-xGex/Si," Applied Physics Letters, Vol. 79, Issue 20 (November 12, 2001), pp. 3344-3346.
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	C49	Li *et al.*, "A Comparison of CMOS and SiGe LNA's and Mixers for Wireless LAN Applications," IEEE 2001 Custom Integrated Circuits Conference, (2001), pp. 531-534.
	C50	Lu *et al.*, "High Performance 0.15 μM Gate-Length P-Type SiGe MODFET's and MOS-MODFET's," IEEE Transactions on Electron Device, Vol. 47, Issue 8 (August 2000), pp. 1645-1652.
	C51	Lukyanchikova *et al.*, "Noise Investigation of SiGe and Si nMOSFET's with Gate Oxide Grown by Low Temperature Plasma Anodisation," IEEE – 2000 High Performance Electron Devices for Microwave and Optoelectronic Applications, (2000), pp. 14-19.
	C52	Maeda *et al.*, "Feasibility of 0.18 μM SOI CMOS Technology Using Hybrid Trench Isolation with High Resistivity Substrate for Embedded RF/Analog Applications," IEEE Transactions on Electron Devices, Vol. 48, Issue 9 (September 2001), pp. 2065-2073.
	C53	Manku *et al.*, "Microwave CMOS – Devices and Circuits," IEEE 1998 Custom Integrated Circuits Conference, (May 1998), pp. 59-66.
	C54	Manku *et al.*, "RF Simulations and Physics of the Channel Noise Parameters Within MOS Transistors," IEEE 1999 Custom Integrated Circuits Conference, (May 1999), pp. 369-372.
	C55	Mathew *et al.*, "Effect of Ge Profile on the Frequency Response of SiGe pFET on Sapphire Technology," Office of Naval Research and IBM Research Division, pp. 130-131.

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OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.		OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
	C56	Mathew *et al.*, "Hole Confinement and Low-Frequency Noise in SiGe PFET's on Silicon-on-Sapphire," IEEE- Electron Device Letters, Vol. 20, Issue 4 (April 1999), pp. 173-175.
	C57	Michelakis *et al.*, "SiGe HMOSFET Differential Pair," IEEE-2001 Circuits and Systems – ISCAS International Symposium, (2001), pp. I679-I682.
	C58	Momose *et al.*, "Ultrathin Gate Oxide CMOS with Nondoped Selective Epitaxial Si Channel Layer," IEEE Transactions on Electron Devices, Vol. 48, Issue 6 (June 2001), pp. 1136-1144.
	C59	Nemirovsky *et al.*, "1/f Noise in CMOS Transistors for Analog Applications," IEEE Transactions on Electron Devices, Vol. 48, Issue 5 (May 2001), pp. 921-927.
	C60	Nishi *et al.*, "Impact of New Materials, Changes in Physics and Continued ULSI Scaling on Failure Mechanisms and Analysis," IEEE 1999 7th IPFA '99 Singapore, (August 1999), pp. 1-8.
	C61	Niu *et al.*, "Noise Modeling and SiGe Profile Design Tradeoffs for RF Applications," IEEE Transactions on Electron Devices, Vol. 47, Issue 11 (November 2000), pp. 2037-2044.
	C62	Niu *et al.*, "RF and Microwave Noise Optimization of UHV/CVD SiGe HBT's," IEEE – 1999 Bipolar/CiCMOS Circuits and Technology Meeting, Vol. 1.2 (April 1999).
	C63	Ohguro *et al.*, "An 0.18 – μM CMOS for Mixed Digital and Analog Applications with Zero-Volt-Vth Epitaxial-Channel MOSFET's," Vol. 46, Issue 7 (July 1999), pp.1378-1383.
	C64	Ohmi *et al.*, "New Paradigm of Silicon Technology," IEEE Proceedings, Vol. 89, Issue 3 (March 2001), pp. 394-412.
	C65	Okhonin *et al.*, "DC and Low-Frequency Noise Characteristics of SiGe P-Channel FET's Designed for 0.13-μM Technology," IEEE Transactions on Electron Devices, Vol. 46, Issue 7 (July 1999), pp. 1514-1517.
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	C68	Park *et al.*, "Body Bias Dependence of 1/F Noise in NMOS Transistors from Deep-Subthreshold to Strong Inversion," IEEE Transactions on Electron Devices, Vol. 48, Issue 5 (May 2001), pp. 999-1001.
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	C70	Pfeiffer *et al.*, "Semiconductor 1/F Noise From Dynamic Coupling of Charge Carriers and Lattice," Journal of Applied Physics, Vol. 90, Issue 7 (October 1, 2001), pp. 3653-3655.
	C71	Rhayem *et al.*, "1/f Noise in Metal – Oxide – Semiconductor Transistor Biased in Weak Inversion," Journal of Applied Physics, Vol. 89, Issue 7 (April 1, 2001), pp. 4192-4194.
	C72	Richey *et al.*, "Scaling Issues and Ge Profile Optimization in Advanced UHV/CVD SiGe HBT's," IEEE – 1996 Bipolar/BiCMOS Circuits and Technology Meeting, (March 1996), pp. 19-22.

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OTHER ART, JOURNAL ARTICLES, ETC.

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	C73	Saito *et al.*, "0.15-μM RF CMOS Technology Compatible with Logic CMOS for Low-Voltage Operation," IEEE Transactions on Electron Devices, Vol. 45, Issue 3 (March 1998), pp. 737-742.
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	C75	Subbanna *et al.*, "Silicon-Germanium BICMOS Technology and a CAD Environment for 2049 GHz VLSi Mixed-Signal ICS," IEEE 2001 Custom Integrated Circuits Conference, (July 2001), pp. 559-566.
	C76	Sugimoto *et al.*, "A 2V, 500 MHz and a 3V, 920 MHv Low-Power Current-Mode 0.6μm CMOS VCO Circuit," Vol. E82-C, Issue 8 (July 1999), pp. 1327-1329.
	C77	Tenbroek *et al.*, "Self-Heating Effects in SOI MOSFETs and their Measurement by Small Signal Conductance Techniques," IEEE Transactions on Electron Devices, Vol. 43, Issue 12 (December 1996), pp. 2240-2248.
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	C80	Wesler *et al.*, "Electron Mobility Enhancement in Strained-Si N-Type Metal-Oxide-Semiconductor Field-Effect Transistors," IEEE Electron Device Letters, Vol. 15, Issue 3 (March 1994), pp. 100-102.
	C81	Wesler *et al.*, "The Application of Strained Silicon/Relaxed Silicon Germanium Heterostructures to Metal Oxide Semiconductor Field-Effect Transistors," PhD Thesis, Stanford University, (1995), pp. 1-205.
	C82	Zeuner *et al.*, "High Frequency SiGe-N-Modfet for Microwave Applications," Vol. 9, Issue 10 (October 1999), pp. 410-412.
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EXAMINER	DATE CONSIDERED